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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/583,617	05/31/2000	Rama R. Goruganthu	AMDA.441PA	2990

7590 08/30/2002

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EXAMINER
SOUW, BERNARD E

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 08/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/583,617	GORUGANTHU ET AL.	
	Examiner	Art Unit	
	Bernard E Souw	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 16 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

- It is unclear whether or not the *region* recited in claim 1, "*exposing a **region of the insulator** of the SOI structure*", is the same as that of claim 20, "*to expose a **BOX portion** of the SOI structure*". Although BOX and SOI are both insulators, the SOI can be turned into active semiconductor layers (source & drain), as shown by Yoshida (USPAT #6,137,295) in the diffusion layers 1e in Fig.1 and Fig.5, to be distinguished from the BOX layer 1c.

To proceed with this Office Action, the BOX layer 1c in claim 20 will be distinguished from the insulator part of the SOI structure, the latter being understood as those parts of the SOI which remain insulator, i.e., the section between the two diffusion regions on the left of the exposed region 1j in Yoshida's Fig.1 and Fig.5. Thus, in Fig.1

the "*insulator part of the SOI structure*" is not exposed. On the other hand, in Fig.5 this part is exposed due to the removal of the BOX layer 1c, resulting in an open region 1j that exposes the insulator parts of the SOI.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Insofar as the Examiner can ascertain beyond the previous rejections of claims 1, 16 and 20 under § 112, second paragraph, claims 1, 2, 8-11, 16-21 and 23 are rejected under 35 U.S.C. 102(a) and 102(e) as being *clearly anticipated* by Yoshida (USPAT #6,137,295).

5. Regarding claims 1, 2, 8-11, and 16-20, Yoshida invents a method for analyzing a semiconductor die (2, 3) having silicon-on-insulator (SOI) structure 1s and a back side opposite circuitry 1f & 1g near a circuit side, as shown in Fig.1 (referring to claim 16) and Fig.5 (referring to claims 1 & 2), the method comprising:

- removing substrate 1a shown in Fig.5 from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure (the section between the two diffusion regions on the left of the exposed region 1j) where the substrate (1a) has been removed (1j), as recited in Col.6/ll.46-57; and
- inducing a detectable response from the exposed region as a function of a portion of the circuitry, as recited in Col.6/ll.51-57. and therefrom, analyzing the die, as recited in Col.5/ll.19-32.

► Regarding claim 2, Yoshida's method of inducing response is by using an electron beam 15 (EB) shown in Fig.2, as recited in Col.5/ll.19-32 & Col.5/ll.53-55.

► Regarding claim 8, Yoshida's detectable response is obtained from source/drain region 1e (S/D = diffusion region) shown in Fig.1 and Fig.5, as disclosed in Col.5/ll.1-5

► Regarding claim 9, the step of using the BOX layer 1c in Fig.1 and Fig.5 as a dielectric in inducing a detectable response is disclosed in Col.6/ll.51-56, i.e., from the absence of secondary electrons thereby detected.

► Regarding claim 10, the step of removing a portion of the substrate 1a to expose a portion of the BOX 1c, as shown in Fig.1 and recited in Col.5/ll.8-32.

► Regarding claim 11, Yoshida's method is a post-manufacturing analysis because the device is analyzed after its manufacture is completed, as recited in Col.6/ll.14-19.

► Claims 16 and 17 are apparatus (system) claims reciting limitations that are already rejected in claim 1. The additional recitation of a detector in claim 17 is shown by Yoshida as numeral 14 in Fig.2.

► Regarding claims 18 and 19, the limitation of using a controller to control the substrate removal in claim 17 is rendered obvious by Yoshida's use of the SOI layer as an etching stop to control the substrate removal process, as recited in Col.6/ll.58-60.

► Specifically regarding claim 20, the limitation that the substrate removal arrangement is adapted to remove enough substrate to expose a BOX portion of the SOI structure is evidenced by Yoshida's result, shown in Fig.1 by numeral 1c (BOX), and recited in Col.5/ll.8-13.

6. Claims 3-7, 12-14 and 21-23 are rejected under 35 U.S.C. 102(a) and 102(e) as being *anticipated* by Yoshida.

► Regarding claim 3, the step of detecting secondary electrons in response to the EB 15 and the portion of the circuitry is recited in Col.5/ll.19-22, whereas the use of a scanning electron microscope (SEM) is conventional and well known in the art. The latter is an Official Notice supported by many published documents, including Talbot et al. (USPAT #6,091,249) in Col.3/ll.13-16 & Col.6/ll.59-60, as well as by Steffan et al. (USPAT #6,200,823 B1) in Col.1/ll.64-67.

► Regarding claim 4, the step of analyzing the die by detecting the difference between the secondary electron signals obtained from two selected circuit portions is shown by the device 1X in Fig.3, which consists of a plurality of circuit portions (1s & 1f) shown in Fig.1 and Fig.5, which represents voltage variations across the plurality of circuit portions, results in a waveform shown in Fig.3, as recited in Col.6/ll.7-11.

► Regarding claims 5 and 21, the step of obtaining an image of the die that represents variations in voltage across the plurality of circuit portions is recited in Col.5/ll.57-63, and shown in Fig.3 and Fig.4.

► Regarding claim 6, the step of using a pulsed EB is disclosed in Col.6/ll.1-6.

► Regarding claim 7, the step of using a coupling power supply and inputting electrical signals to the die to generate a response is inherent in Yoshida's, as implicated by the testing set 11 shown in Fig.2, recited in Col.5/ll.53-60, which inherently and conventionally includes a power supply.

► Regarding claim 12, the electrical stimulus applied to the circuitry in the die is provided by the DUT board 12 shown in Fig.2, recited in Col.5/ll.43-48.

► Regarding claim 13, whether or not to stimulate a response by using the DUT board 12, until a failure is induced in the die, is a mere matter of deliberate choice . As such, the step is unpatentable for only involving routine skill in the art.

► The limitation of claim 14 is basically an automation of a step, or method, which is normally implemented manually. It would have been obvious to one having ordinary skill in the art at the time the invention was made to put the input signals in a continuous loop, since it has been held that broadly providing a mechanical or automatic means to replace manual activity which has accomplished the same result involves only routine skill in the art. *In re Venner*, 120 USPQ 192.

► Regarding claim 22, the limitation that the image of the die shows light and dark areas, the dark areas being indicative of circuit portions having positive voltage greater that that of the lighter areas, is well known in the art. this Official Notice is supported by

a large number of prior arts, e.g., by Talbot et al. (USPAT #6,091,249) in the Abstract/ll.1-19 and in Col.6/ll.46-48, shown in Fig.3a-d, by Kim et al. (USPAT #2002/0043628A1) in the Abstract/ll.1-6 from bottom.

► Regarding claim 23, the step of using a tester adapter to introduce electrical stimulus to the die is disclosed in testing set 11 shown in Fig.2, as recited Col.5/ll.53-60.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Talbot et al. (USPAT #6,019,249) and Steffan et al. (USPAT #6,200,823 B1).

8. Yoshida shows all the limitations of claim 5, as previously applied to the parent claim 1, except the recitation of using a non-defective die as a reference. Talbot et al. disclose a method for analyzing a semiconductor die using an electron beam from a SEM 20 shown in Fig.1, as recited in Col.5/ll.33-57. Talbot's apparatus and method use a defect-free device as reference, as recited in Col.6/ll.65-67.

It would have been obvious to adopt Talbot's use of a non-defective die as a reference in Yoshida's method, since from a single image of a device alone *in the absence of other information*, it is difficult to determine whether or not the device under testing (DUT) contains an error, as implicated by Talbot et al. in Col.6/ll.63-65.

One would have been motivated to compare the EB image of a DUT with a known, non-defective device, as used by Talbot et al., since a defective die would be much more easily and much more quickly recognized by an operator, especially when the image of the non-defective die is subtracted from the currently measured image of a DUT (die under testing), thus highlighting the defect, as suggested by Steffan et al. in Col.3/ll.8-13.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bernard E Souw whose telephone number is 703 305 0149. The examiner can normally be reached on Monday thru Friday, 9:00 am to 5:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R Lee can be reached on 703 308 4116. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872 9318 for regular communications and 703 872 9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

bes
August 23, 2002

JOHN R. LEE
SUPERVISORY PATENT EXAMINER
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